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ABSTRACT: Tri-gate transistors offer better performance than planar transistors by exerting additional gate control over a channel from two lateral sides of semiconductor nanowalls (or "fins"). Here we report the bottom-up assembly of aligned CdS nanowalls by a simultaneous combination of horizontal catalytic vapor-liquid-solid growth and vertical facet-selective noncatalytic vapor-solid growth, and their parallel integration into tri-gate transistors and photodetectors at wafer scale (cm^2) without post-growth transfer or alignment steps. These tri-gate transistors act as enhancement-mode transistors with an on/off current ratio on the order of 10^8, four orders of magnitude higher than the best results ever reported for planar enhancement-mode CdS transistors. The response time of the photodetector is reduced to sub-microsecond, one order of magnitude shorter than the best results ever reported for photodetectors made of bottom-up semiconductor nanostructures. Guided semiconductor nanowalls open new opportunities for high-performance 3D nanodevices assembled from the bottom up.

■ INTRODUCTION

Three-dimensional (3D) nanodevices are expected to provide more compact and efficient components than traditional planar (2D) nanodevices for future generations of semiconductor chips.[1-6] For example, Intel's 2011 innovation of 3D tri-gate field-effect transistors (tri-gate FETs or FinFETs) enabled transistor scaling down to 22 nm, which was the first break of the scaling limit (32 nm) reached by conventional planar architecture.[7] Five years later, Samsung Electronics announced mass production at 10 nm using FinFETs. Unlike planar FETs, in which gate control is only exerted on top of the belt-like channel, the gate electrode in tri-gate FETs is wrapped around three faces (the top and two lateral sides) of a vertical fin channel,[6-9] allowing most of the surface area for electrostatic control without increasing gate size. Semiconductor fins or nanowalls (i.e. nanoribbons standing with their narrow facets on the surface, like a wall on the ground) are the building blocks for conducting channels in tri-gate FETs. To date, on one hand, commercial silicon tri-gate FET fins[7] and nanowalls of other tri-gate FETs under investigation[8-11] have been fabricated top-down. On the other hand, although a few semiconductor nanowalls have been obtained via bottom-up approaches,[12-17] they have not yet been employed to build tri-gate FETs.

Inspired by building brick walls in daily life, we realized that nanowalls could form spontaneously from the bottom up by a simultaneous combination of horizontal growth and vertical facet-selective growth. Horizontal growth can be achieved by the catalytic vapor-liquid-solid (VLS) mechanism, where nanowire growth occurs from nucleated seeds at a liquid-solid interface. This proceeds with the help of a liquid alloy which rapidly absorbs vapor species to supersaturation levels.[18] VLS growth usually leads to freestanding or vertically-aligned semiconductor nanowires, depending on the lattice match between nanowires and substrates.[19-21] Recently, VLS growth of horizontally aligned nanowires has been demonstrated by several groups.[13,22,23] So far, a growing list of semiconductors, such as GaAs,[22] TiO_2,[24] GaN,[23,25-27] ZnO,[13,14,28,29] ZnSe,[30] ZnTe[17] and CdSe,[31] have proved to enable horizontal growth of self-aligned nanowires on flat or faceted substrates. A non-catalytic vapor-solid (VS) growth mechanism, where crystal growth occurs on the nanowire surface owing to the accumulation of surface-adsorbed atoms in vapor atmosphere, can take place simultaneously with the VLS growth, leading to freestanding tapered nanoribbons.[32-34] The rate of VS growth is closely related to surface energy,[32-34] resulting in a facet-selective growth.[35,36] Specifically, vertical facet-selective growth is expected to be achieved by the VS growth as long as the top surfaces of VLS-catalytic horizontal nanowires have higher surface energies than those of the lateral sides. This can be exploited for the bottom-up growth of nanowalls.

Here we report the growth of self-aligned CdS nanowalls with high single-crystal quality on flat or faceted sapphire surfaces. Structural characterization reveals that CdS nanowalls grow epitaxially along certain crystal orientations on flat sapphire surfaces while graphoepitaxy (i.e. growth along relief features larger than lattice parameters[23,37]) is preferred on faceted sapphire surfaces with nanogrooves or nanosteps. These self-aligned nanowalls were integrated in parallel into tri-gate FETs and photodetectors in a scalable manner without post-growth transfer or alignment steps. The achieved tri-gate FETs were enhancement-mode (E-mode) FETs with a ~10^8 on/off current ratio, four orders of magnitude higher than the best results ever reported for planar E-mode CdS FETs.[38] Moreover, the photodetectors exhibit a sub-microsecond response at room temperature, one order of magnitude faster than the best results ever reported for photodetectors made of bottom-up compound semiconductor nanostructures.[31]

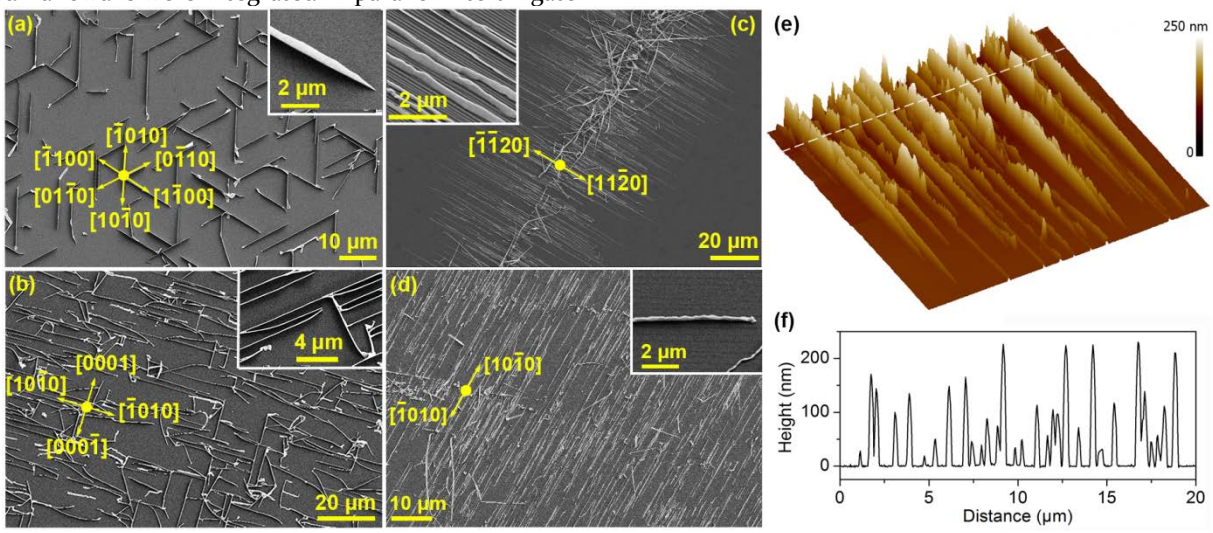

Figure 1. Guided CdS nanowalls on different sapphire surfaces. SEM of guided CdS nanowalls on well-cut flat C(0001) (a), A(11$\bar{2}$0) (b), annealed M(10$\bar{1}$0) (c) and annealed miscut C(0001) sapphire surfaces (d). The yellow arrows in each panel show the crystallographic orientations of the sapphire. The insets in panels (a), (c), and (d) show the nanowall geometry at views tilted by 30°. (e) 3D AFM image of CdS nanowalls on the annealed M(10$\bar{1}$0) sapphire surface, where the scanning size was 21.6 × 21.6 μm². (f) Representative nanowall height along the dashed line in (e).

■ RESULTS AND DISCUSSION

The equilibrium Wulff shape of sapphire is characterized by C(0001), R(1$\bar{1}$02), S(10$\bar{1}$1), P(11$\bar{2}$3), A(11$\bar{2}$0), and M(10$\bar{1}$0) facets, in order of increasing surface energy.[23] Figure 1 shows SEM views of guided CdS nanowalls on four different sapphire surfaces. Guided CdS nanowalls on flat C(0001) sapphire surfaces formed triangular networks (Figure 1a) when dispersed gold nanoparticles were used as growth catalysts. On flat A(11$\bar{2}$0) sapphire surfaces, CdS nanowalls grew orthogonally along the $\pm[0001]_{Al2O3}$ and $\pm[10\bar{1}0]_{Al2O3}$ directions (Figure 1b). On annealed M(10$\bar{1}$0) sapphire with V-shaped nanogrooves (inset and Figure S1),[23,27,30] CdS nanowalls were self-aligned along the nanogrooves in the $\pm[11\bar{2}0]_{Al2O3}$ directions (Figure 1c). L-shaped nanosteps were obtained by annealing the C(0001) sapphire miscut by 2° toward $[11\bar{2}0]_{Al2O3}$. Unlike the six alignment directions of the CdS nanowalls on flat C(0001) sapphire surfaces, the CdS nanowalls on the miscut C(0001) sapphire surfaces were aligned only along the $\pm[10\bar{1}0]_{Al2O3}$ directions (Figure 1d).

Although guided CdS nanowalls were obtained on four sapphire surfaces, we found that the nanowalls on annealed M(10$\bar{1}$0) sapphire surfaces had the largest length (exceeding 70 μm, Figure S2) and the highest density (up to 30 nanowalls per 10 μm, Figure S3), making them a good choice for integration into nanodevices. The AFM image of guided CdS nanowalls on annealed M(10$\bar{1}$0) sapphire surfaces (Figure 1e) reveals that the heights of the nanowalls usually decrease gradually toward the nanowall ends (i.e. away from the initial location of the catalyst) and have typical values in the range of 50–200 nm (Figure 1f).

Epitaxially guided nanowalls on C(0001) sapphire

Low-magnification transmission electron microscope (TEM) views (Figures 2a, 2b) confirm that the guided CdS nanostructures on C(0001) sapphire surfaces have a well-defined nanowall geometry. Corresponding fast Fourier transformation (FFT) patterns reveal that all examined nanowalls possess a wurtzite structure but two different crystallographic growth axes. Four nanowalls grew along

the nonpolar $[10\bar{1}0]_{CdS}\|[10\bar{1}0]_{Al2O3}$ axis (Figure 2c), and the other two grew along the polar $[0001]_{CdS}\|[10\bar{1}0]_{Al2O3}$ axis (Figure S4). For nanowalls grown along the $[10\bar{1}0]_{CdS}$ axis, the transversal and horizontal planes were $\pm(1\bar{2}10)_{CdS}$ and $\pm(0001)_{CdS}$ planes, in parallel with $\pm(1\bar{2}10)_{Al2O3}$ and $\pm(0001)_{Al2O3}$ planes, respectively (Figures 2a, 2d). The theoretical mismatch across the nanowall at the CdS/Al_2O_3 interface was -13%, indicating many misfit dislocations at the CdS/Al_2O_3 interface (pink arrows in Figure 2e). The distance between two adjacent misfit dislocations was about eight CdS planes and seven Al_2O_3 planes, as shown in the Fourier-filtered image of the CdS/Al_2O_3 interface (Figure 2e). On the basis of the above analyses, the growth model and the crystallographic orientations of the CdS nanowalls on C(0001) sapphire surfaces is shown schematically in Figure 2f.

Epitaxially guided nanowalls on A$(11\bar{2}0)$ sapphire

Guided CdS nanostructures on A$(11\bar{2}0)$ sapphire surfaces also have a well-defined nanowall geometry (Figures 3a and 3b). The height-to-width aspect ratio of the nanowalls exceeds 10 (i.e. 24 nm in width and 248 nm in height, Figure 3a). Corresponding FFT patterns reveal that some nanowalls grew along the $[0001]_{CdS}\|[10\bar{1}0]_{Al2O3}$ axis, with $(11\bar{2}0)_{CdS}\|(0001)_{Al2O3}$ transversal planes and $(10\bar{1}0)_{CdS}\|(11\bar{2}0)_{Al2O3}$ horizontal planes (Figure S5), while others grew along the $[1\bar{1}02]_{CdS}\|[10\bar{1}0]_{Al2O3}$

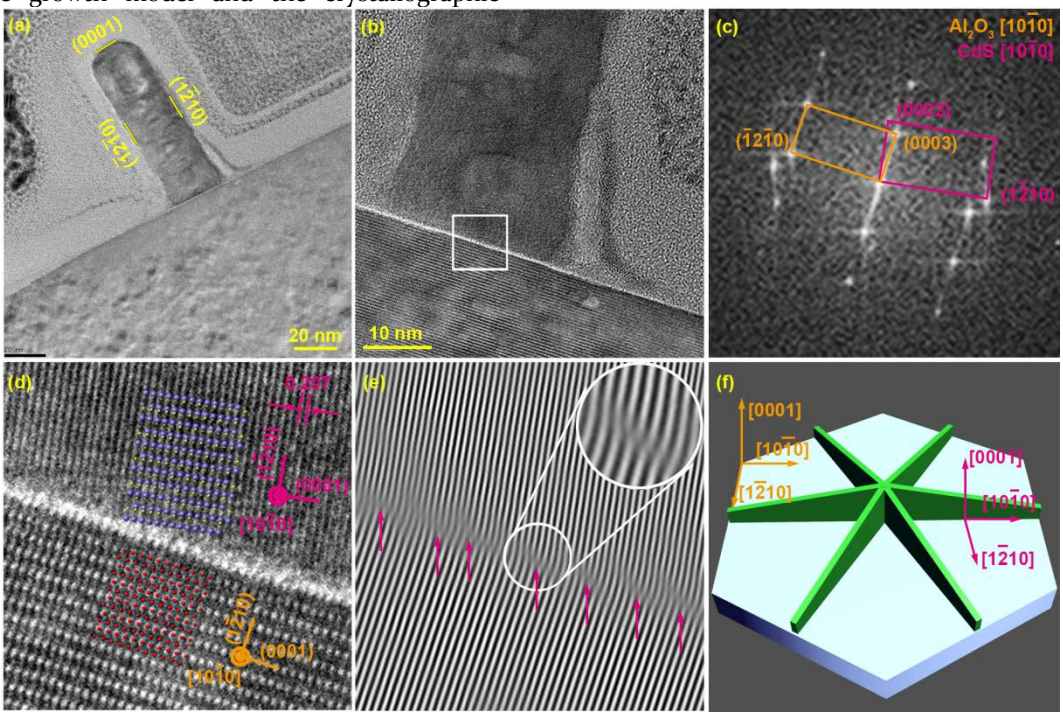

Figure 2. Structural characterization of guided CdS nanowalls on a flat C(0001) sapphire surface. (a, b) Cross-sectional TEM views, (c) FFT image and (d) magnified view of the area enclosed by the white contour in (b) with crystallographic orientations and atomic models, and (e) A Fourier-filtered image highlighting misfit dislocations (inset) at the CdS/Al_2O_3 interface. (f) Proposed growth model.

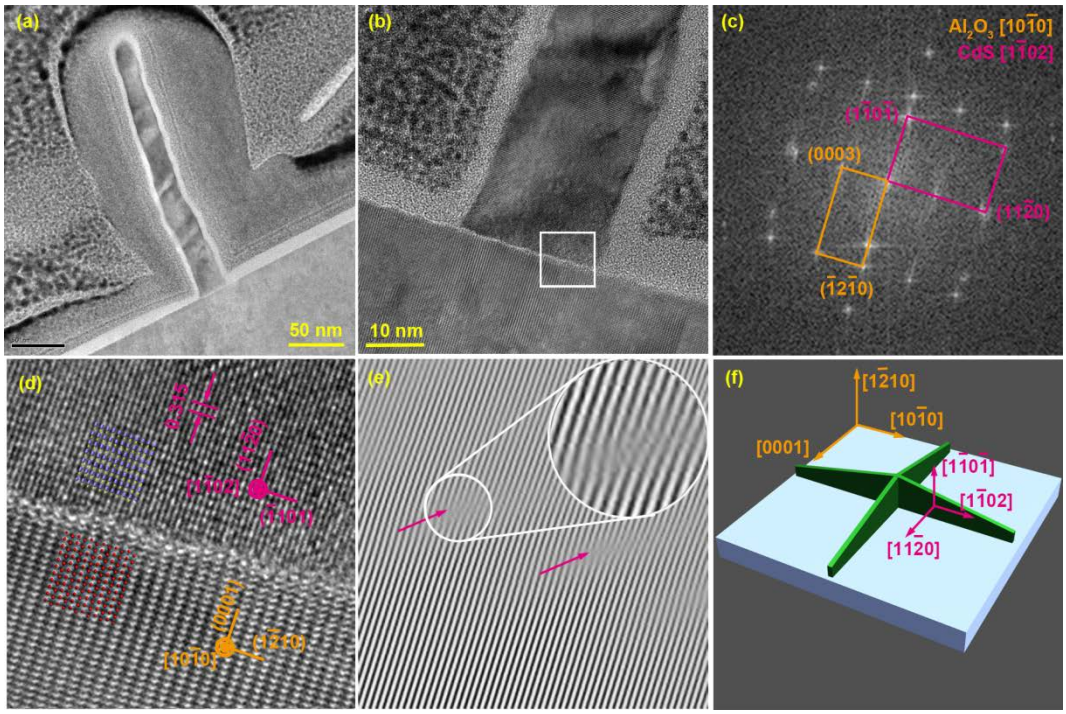

Figure 3. Structural characterization of guided CdS nanowalls on a flat A(11$\bar{2}$0) sapphire surface. (a, b) Cross-sectional TEM views, (c) FFT image, and (d) magnified view of the area enclosed by the white contour in (b) with crystallographic orientations and atomic models. (e) A Fourier-filtered image highlighting the misfit dislocations (inset) at the CdS/Al_2O_3 interface. (f) Proposed growth model.

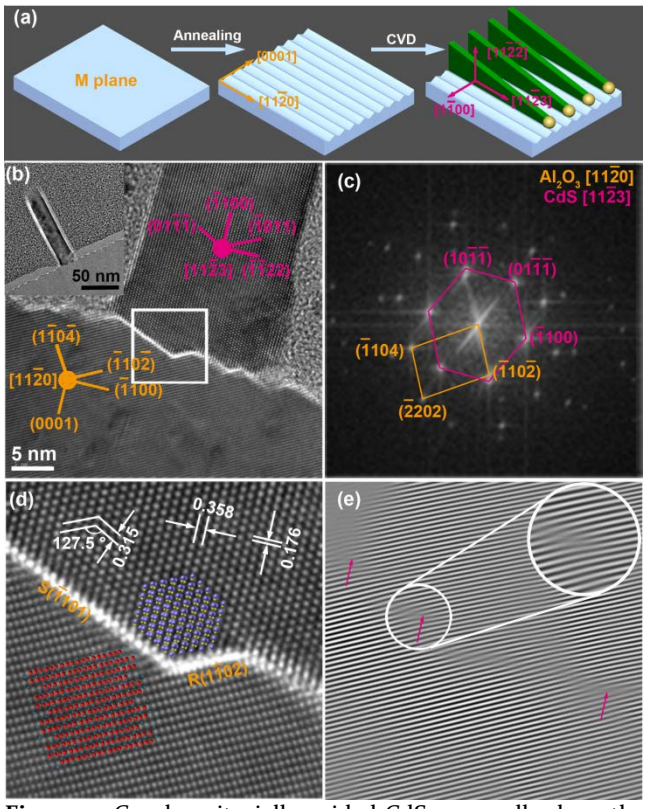

Figure 4. Graphoepitaxially guided CdS nanowalls along the nanogrooves of annealed M(10$\bar{1}$0) sapphire. (a) Schematic drawing of graphoepitaxial growth, (b) cross-sectional TEM views, (c) FFT image of panel (b), (d) magnified view of the white box marked area in (b) with crystallographic orientations and atomic models, and (e) Fourier-filtered image highlighting periodic dislocations (inset) at the CdS/Al_2O_3 interface.

axis (Figure 3c) with $(1\bar{1}0\bar{1})_{Al2O3}\|(11\bar{2}0)_{Al2O3}$ horizontal planes (Figure 3d). The Fourier-filtered image at the CdS/Al_2O_3 interface (Figure 3e) shows that the distance between two adjacent misfit dislocations was about 24 CdS planes and 23 Al_2O_3 planes, which is equal to the spacing expected from a simple calculation of the matching between the $(11\bar{2}0)_{CdS}$ planes and $(0006)_{Al2O3}$ planes. The growth model and crystallographic orientations of the CdS nanowalls on A(11$\bar{2}$0) sapphire surfaces is shown in Figure 3f.

Graphoepitaxially guided nanowalls along the nanogrooves of annealed M(10$\bar{1}$0) sapphire

As schematically shown in Figure 4a, V-shaped nanogrooves can be obtained by annealing M(10$\bar{1}$0) sapphire. All CdS nanowalls on annealed M(10$\bar{1}$0) sapphire surfaces investigated by TEM have the same axis along $[11\bar{2}3]_{CdS}\|[11\bar{2}0]_{Al2O3}$ (Figures 4b and 4c). The $[11\bar{2}3]_{CdS}$ axis has rarely been reported for CdS and other

compound semiconductor nanostructures. Possible reasons for the selectivity of $[11\bar{2}3]_{CdS}$ are discussed in the paragraphs on the growth mechanism. The transversal and horizontal planes of CdS nanowalls on annealed $M(10\bar{1}0)$ sapphire surfaces were $(\bar{1}100)_{CdS}$ and $(11\bar{2}\bar{2})_{CdS}$, in parallel with $(0001)_{Al2O3}$ and $(\bar{1}100)_{Al2O3}$ planes, respectively. On the basis of the FFT pattern

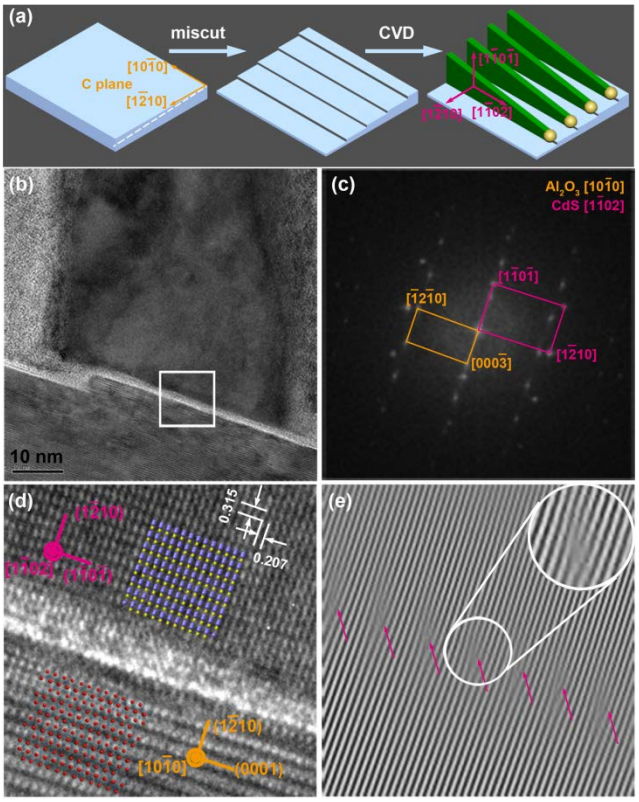

Figure 5. Graphoepitaxially guided CdS nanowalls along the nanosteps of annealed miscut C(0001) sapphire. (a) Schematic drawing of graphoepitaxial growth, (b) cross-sectional TEM view, (c) FFT image of panel (b), (d) magnified view of the white box marked area in (b) with crystallographic orientations and atomic models, and (e) Fourier-filtered image highlighting periodic dislocations (inset) at the CdS/Al_2O_3 interface.

and atomic model of wurtzite CdS (Figure 4d), we deduce that the top facets of the CdS nanowalls on annealed $M(10\bar{1}0)$ sapphire surfaces were most likely composed of $\{10\bar{1}\bar{1}\}_{CdS}$ planes at an angle of 127.5°. The FFT pattern in Figure 4c also indicates that the $\{10\bar{1}\bar{1}\}_{CdS}$ planes had the smallest misfit dislocations with the $R(1\bar{1}02)_{Al2O3}$ planes. The lattice mismatch between $\{10\bar{1}\bar{1}\}_{CdS}$ and $R(1\bar{1}02)_{Al2O3}$ was 9%, leading to considerable misfit dislocations at the CdS/Al_2O_3 interface (Figure 4e).

Graphoepitaxially guided nanowalls along the nanosteps of annealed miscut C(0001) sapphire

Figure 5a shows schematically that L-shaped nanosteps were obtained by annealing the miscut C(0001) sapphire. Both SEM (Figure 2d) and TEM images (Figure 5b) show that CdS nanowalls grew along the nanosteps, instead of the six directions of the flat C(0001) sapphire surfaces. FFT patterns reveal that CdS nanowalls on miscut C(0001) sapphire surfaces had the same axis of $[1\bar{1}02]_{CdS} \parallel [10\bar{1}0]_{Al2O3}$ with transversal planes of $(1\bar{2}10)_{CdS} \parallel (1\bar{2}10)_{Al2O3}$ and horizontal planes of $(1\bar{1}0\bar{1})_{CdS} \parallel (0001)_{Al2O3}$ (Figures 5c and 5d). The smallest lattice mismatch found between $(1\bar{2}10)_{CdS}$ and $(1\bar{2}10)_{Al2O3}$ was -13%, the same as that of the guided nanowalls on flat C(0001) sapphire surfaces; therefore, numerous misfit dislocations were found at the CdS/Al_2O_3 interface (Figure 5e).

The above TEM results suggest that the guided CdS nanowalls possessed a high single-crystalline quality, which is consistent with the results of X-ray diffraction (XRD, Figure S6 and Table S1) and photoluminescence (PL, Figure S7). Except for CdS nanowalls on the annealed $M(10\bar{1}0)$ sapphire surfaces, all nanowalls on the flat C(0001), $A(11\bar{2}0)$, and miscut C(0001) sapphire surfaces shared the same $\{11\bar{2}0\}_{CdS}$ transversal planes (Table S2). This is consistent with the fact that the $\{11\bar{2}0\}_{CdS}$ planes have the lowest surface energy for wurtzite CdS (0.58 J/m^2);[39] consequently, $\{11\bar{2}0\}_{CdS}$ planes are the most stable surfaces and usually appear as facets of the equilibrium morphology for wurtzite CdS.[39] The possible reason that CdS nanowalls on annealed $M(10\bar{1}0)$ sapphire have different transversal planes is discussed below.

Growth mechanism

Underlying mechanisms causing formation of free-standing nanobelts have been proposed by several groups.[40,41] However, the mechanism for in-plane nanostructure growth remains under discussion.[24] There are several processes proposed for the growth of free-standing nanobelts in an evaporation route, including the VLS mechanism,[18] VS mechanism,[40] oxide-assisted growth,[41] and surface-energy-induced growth.[41] In our case, oxide-assisted growth can be excluded since no oxide was used and growth proceeded under a N_2 atmosphere. The observation of a metal nanoparticle at the end of each nanowall (Figure S1) indicates that the growth of guided nanowalls proceeded by the VLS mechanism.[18] Observations of sawtooth-like rough top surfaces and gradually decreasing heights toward the ends of nanowalls (Figure 1e and Figure S8) indicate simultaneous vertical growth via the VS mechanism[40] in addition to horizontal propagation via the VLS mechanism.

The growth model for guided CdS nanowalls on the annealed $M(10\bar{1}0)$ sapphire surface is illustrated in Figure 6. The growth of CdS nanowalls was triggered by rapid horizontal VLS growth along nanogrooves. Owing to the restriction of the $R(1\bar{1}02)$ and $S(10\bar{1}1)$ facets of the underlying V-shaped nanogrooves, the $[11\bar{2}3]_{CdS}$ axis was

selected to reduce the lattice mismatch of CdS with the R($1\bar{1}02$) and S($10\bar{1}1$) sapphire planes.[24] Because of the $[11\bar{2}3]_{CdS}$ growth axis, the top facets of the CdS nanowalls were $\{10\bar{1}\bar{1}\}_{CdS}$ and the transversal planes were $\{10\bar{1}0\}_{CdS}$ (inset in the lower right). All the newly formed surfaces further adsorb atoms from high-concentration precursors and nucleate at rough sites (i.e. atomic steps and screw dislocations) to start growth via the VS mechanism. Since the surface energy of $\{10\bar{1}0\}_{CdS}$ planes is much lower than that of $\{10\bar{1}\bar{1}\}_{CdS}$ planes,[39] the adsorbed atoms preferentially diffuse to the more chemically active $\{10\bar{1}\bar{1}\}_{CdS}$ surfaces, leading to the faster growth along the top $\{10\bar{1}\bar{1}\}_{CdS}$ surfaces than along the lateral $\{10\bar{1}0\}_{CdS}$ surfaces. For CdS nanowalls on flat C(0001) and A($11\bar{2}0$) as well as miscut C(0001) sapphire surfaces, nanowalls shared the same $\{11\bar{2}0\}_{CdS}$ lateral surfaces (Table S2). Owing to the lowest surface energy of $\{11\bar{2}0\}_{CdS}$ planes,[39] VS growth of CdS along lateral surfaces is slower than along the top as well, which eventually leads to

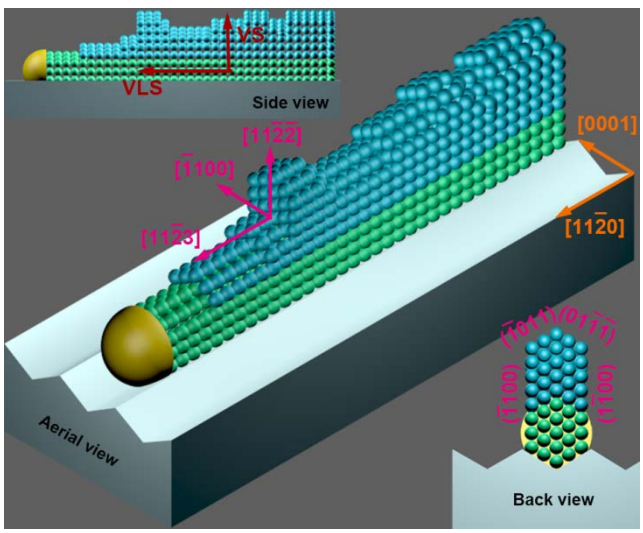

Figure 6. Growth model of CdS nanowalls on the annealed M($10\bar{1}0$) sapphire surface. Green spheres represent atoms precipitated by the VLS process while blue spheres represent the atoms accumulated by the VS process.

formation of CdS nanowalls. The bottom-up growth mechanism of CdS nanowalls is exactly as proposed in the Introduction.

Tri-gate FETs

By taking advantage of the large length, high density, and good alignment of guided CdS nanowalls, nanodevices are expected to be fabricated at wafer scale without post-growth transfer or alignment steps, with each device to be made of many nanowalls. For example, photodetectors were fabricated in large numbers by directly laying down two separated electrodes on the two ends of guided nanowalls. For FET fabrication, the only additional steps are deposition of a dielectric layer followed by deposition of a gate electrode between source and drain electrodes. It is interesting to note that the guided nanowalls on the four different substrates exhibit similar geometry and single-crystal quality (confirmed by HRTEM), therefore the choice of substrate is not expected to have significant influence on the device performance.

Figure 7a shows the SEM of a tri-gate FET made of five CdS nanowalls on an annealed M($10\bar{1}0$) sapphire surface. The cross-sectional TEM view of the gate region (Figure 7b) shows that the gold electrode was wrapped around three facets of the nanowall, thereby realizing a tri-gate configuration. The gate leakage current (I_g) increased linearly to 4 pA as gate voltage (V_g) swept from 0 to 21 V and further increased exponentially as V_g exceeded 21 V (Figure 7c), suggesting that the 50-nm-thick (estimated from Figure 7b) Al_2O_3 layer serves as a good dielectric layer for CdS nanowall tri-gate FETs as long as V_g is less than 21 V.

From the output characteristics in Figure 7d, the source-drain current (I_{ds}) increased linearly at low source-drain voltage (V_{ds}) and further reached a plateau at high V_{ds} for a given V_g. Both the saturated (transistor on state) current and channel conductance (slope of the linear part of each curve) increased drastically with V_g, indicating that these tri-gate FETs are of the n-channel type. A positive threshold voltage (V_{th}) of ~3.5 V (Figure 7e, brown dashed line) was derived by fitting the high-slope region of the transfer

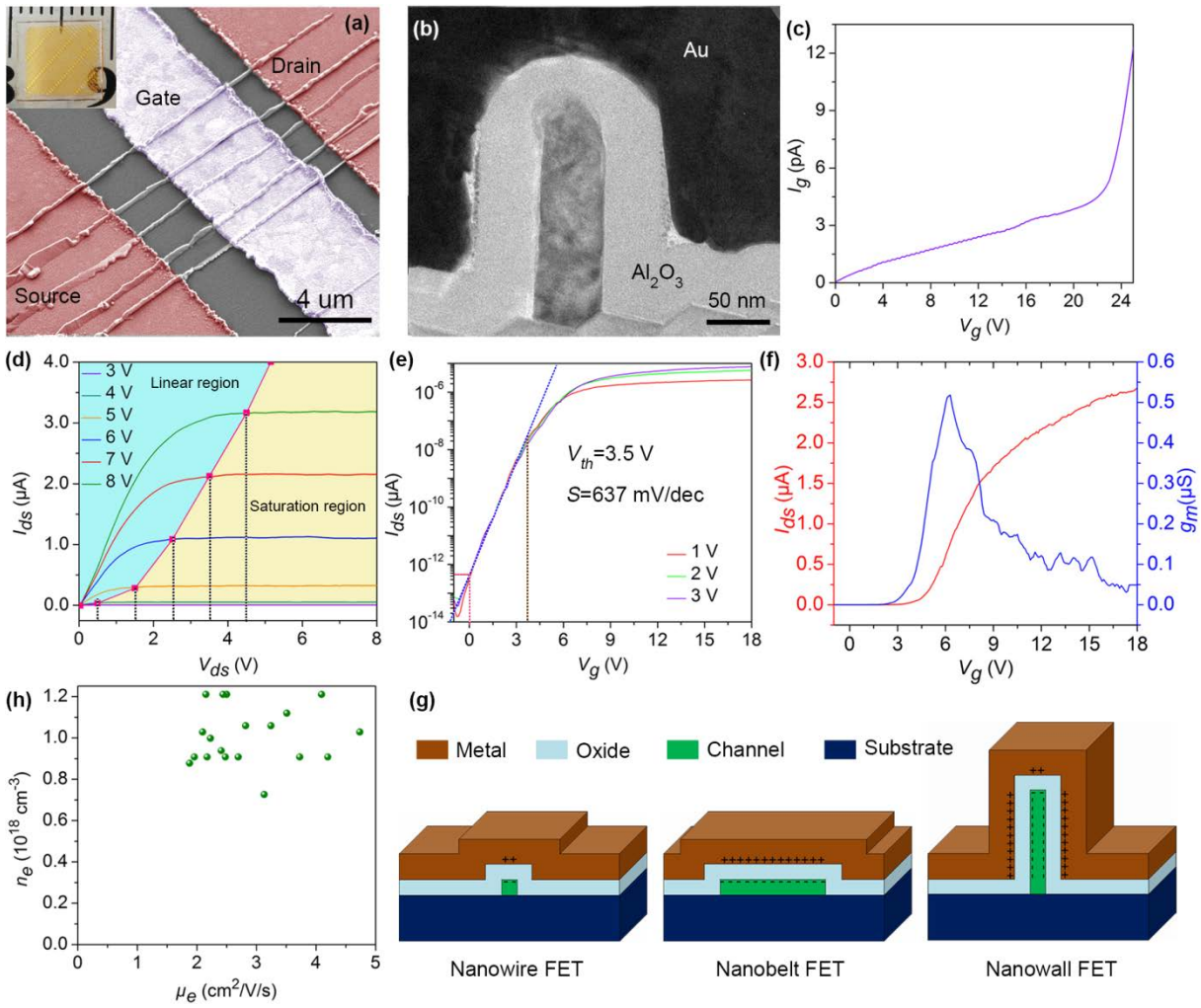

Figure 7. Performance of CdS-nanowall tri-gate transistors. (a) SEM of tri-gate FET made of five CdS nanowalls where false color was added to show the electrodes. The inset shows the digital photograph of the real device with a large number of FETs on the sapphire surface, and the size of the sapphire was 8 × 8 mm². (b) Cross-sectional TEM view of the gate region. (c) Gate leakage current (I_g) vs gate voltage (V_g) at a source-drain voltage (V_{ds}) of 1 V. (d) Output characteristics at various V_g. The boundary between linear (or "Ohmic", blue) and saturation (or "active", yellow) modes is indicated by the pink parabola. The dashed lines indicate the values of V_g-V_{th}. (e) Transfer characteristics at various V_{ds}. (f) Transconductance (g_m, blue) as a function of V_g at V_{ds}=1 V. Corresponding transfer characteristics (I_{ds}, red) are also plotted on a linear scale. (g) Schematic drawing of a planar nanowire FET, nanobelt FET, and tri-gate nanowall FET. (h) Electron mobility (μ_e) *vs* concentration (n_e) for 20 FETs.

characteristics on a logarithmic scale (Figure 7e, blue dashed line); thereby, the tri-gate FETs were E-mode (normally-off) FETs. The transfer characteristics (Figure 7e) show that the on and off currents were ~10^{-6} A and ~10^{-14} A, respectively; hence, an on/off current ratio on the order of 10^8 was achieved. The on/off current ratio was four orders of magnitude higher than the best results ever reported for planar E-mode CdS FETs (6×10^4 at V_{ds}=1 V).[38] In addition to the high on/off current ratio, the standby current (I_{ds} at V_g=0 V) was ~3×10^{-13} A (Figure 7e, marked by the pink dashed line), three orders of magnitude lower than that of planar E-mode CdS FETs (~10^{-10} A).[38] Low standby current is important for reducing FET power consumption.[42-44] The subthreshold swing (S) (Figure 7e) and transconductance (g_m) (Figure 7f, blue) derived from the transfer characteristics at V_{ds}=1 V were 637 mW/dec and 0.52 μS, respectively. Therefore, the electron mobility (μ_e) and electron concentration (n_e) of CdS nanowalls were estimated to be about 3.2 cm²/(V·s) and 1.1×10^{18} cm^{-3}, respectively (see calculation details in the Supporting Information). Averaging over 20 devices, the tri-gate FETs had V_{th}=2.4–4.0 V and an on/off current ratio of 3.3×10^7–3.2×10^8, g_m=0.25–0.65 μS, S=442–833 mV/dec at V_{ds}=1 V, μ_e=1.9–4.7 cm²/(V·s), and n_e=7.3×10^{17}–1.2×10^{18} cm^{-3} (Table S3).

The achievement of E-mode FETs with high on/off current ratio is attributed to the small width of these nanowalls and the tri-gate configuration. Previous work

has demonstrated that planar FETs made of bottom-up nanostructures work in E-mode as long as the thickness of a nanostructure is smaller than its depletion layer width (W_m).[38] Using the measured average n_e (~1.0×10^{18} cm^{-3}), the W_m of CdS nanowalls with gold was ~21 nm considering a planar configuration for the calculation (see details in the Supporting Information). In our case, however, the gate wrapped around three faces of the nanowalls; hence, the total W_m is expected to double (~42 nm, where the contribution from the top face is negligible considering the large height-to-width ratio of the nanowall). As confirmed by cross-sectional TEM, most guided CdS nanowalls (17 out of 21, confirmed by TEM) had widths of 15–35 nm, smaller than W_m; hence, E-mode FETs were achieved.

The 3D tri-gate configuration also enhances electrostatic control of conducting channels by opening most of the nanowall covered by the gate for electron transport at a positive gate voltage.[9] As shown in Figure 7g, for FETs made of semiconductor nanowires or nanobelts, only the top surface of the nanostructure acts as an active gate region (marked with "-"). The situation for the nanowall tri-gate FETs, however, is quite different: most of the nanowall surface can act as an active gate region. A simple calculation suggests how the tri-gate configuration significantly increases the active gate region; For example, the width and height of the nanowalls in Figure 7b were around 50 and 200 nm, respectively, and the thickness of the oxide layer was 50 nm; therefore, 70% of the nanowall surface wrapped by the gate electrode acted as an active gate region. Meanwhile, for the nanowire and nanobelt of similar sizes, only 25% and 40% of the surface, respectively, served as an active gate region.

Unlike the significantly increased on/off current ratio, the electron mobilities of these tri-gate FETs were two orders of magnitude lower than the electron Hall mobility of bulk CdS at room temperature (340 $cm^2/V/s$). The significantly reduced electron mobility indicates strong carrier scattering.[38,45-48] As shown in Figure 7h, there is little electron mobility dependence on carrier concentration. This observation suggests that scattering processes related to unintentional dopants (ionized impurity scattering) can be excluded.[45] We believe that the increased scattering originates from two factors. One is the scattering caused by the interface states between the Al_2O_3 dielectrics and the semiconductor conductive channel (CdS nanowalls), as has often been observed for FETs with a high-κ dielectric layer by other groups.[38,46] The other is the surface roughness scattering caused by interfacial disorder.[47,48] Although the sidewalls of guided nanowalls are nearly flat on an atomic level (Figure 5b), the top surfaces are not. As seen in the SEM (Figure S8) and AFM (Figure 1e), CdS nanowalls have sawtooth-like top surfaces. Further studies clarifying the origin of the scattering are underway. The subthreshold swing of these tri-gate FETs (~650 mV/dec) was two orders of magnitude faster than that of back-gate planar CdS FETs (tens of V/dec),[21,38] which is attributed to the thin dielectrics (50 nm Al_2O_3).

The achievement of E-mode FETs with high on/off current ratio from bottom-up semiconductor nanostructures is important for the following reasons: (i) E-mode FETs are expected to be used in applications such as power amplifier circuits, switching-mode power electronics systems, and high-temperature digital circuits.[49] However, development of high-performance E-mode FETs from bottom-up semiconductor nanostructures remains a challenge owing to the difficulty of achieving low on-resistance and low off-state drain leakage current simultaneously.[8] To our knowledge, most reported FETs made of bottom-up semiconductor nanostructures are D-mode FETs.[38,45,50-52] (ii) A high on/off current ratio is a figure of merit even more critical than high mobility in some practical applications, such as memory, logic circuits, and active matrix displays,[38,42,44] where the off-current should be as low as possible to reach a high contrast ratio and to minimize power consumption in the off-state. To date, although a few examples of E-mode CdS FETs have been presented,[38] the on/off current ratio is limited to 6×10^4, four orders of magnitude lower than that of depletion-mode CdS FETs. Another advantage of 3D tri-gate FETs from guided nanowalls is that the current drive of a device can be increased simply by increasing the number of nanowalls. In addition, superior electrical performance could be archived if the standing nanowalls can be carefully maintained during the device processing.

Sub-microsecond photodetectors

Figure 8a shows an SEM image of a representative photodetector made of eight guided CdS nanowalls on an annealed M($10\bar{1}0$) sapphire surface. The linear characteristic of the photocurrent under different light intensities (Figure 8b) confirms the Ohmic contact between the Cr/Au electrodes and the guided nanowalls. The conductance (G) increased by six orders of magnitude from 2×10^{-12} A/V in the dark condition (inset in Figure 8b) to 1.5×10^{-6} A/V with a laser intensity of 2 W/cm^2 (Figure 8b, pink), indicating very high responsivity for the CdS nanowall photodetector. The increased conductance with laser power density (P) (Figure 8c) can be fitted into a simple power-law function, $G = AP^{\theta}$, where A is a constant for a certain wavelength and θ is an index of photocurrent response to light intensity. The fitted θ is 0.75, which is close to the reported values for CdS-nanoribbon photodetectors[43] and lies in the range of the theoretical prediction of the Rose model (0.7–0.9 for CdS).[53,54] The agreement between the fitted and theoretical θ indicates that photoconductance was related to electron-hole generation, trapping, and recombination within the semiconductor.[55]

Response time is a key parameter that represents the capability of a photodetector to follow a fast-varying optical signal. Figure 8d shows that the photocurrent response of guided CdS nanowalls to a modulated laser is ultra-fast with good stability and repeatability. The time step was set to 25 ns to determine the rise time (t_r) and fall time (t_d). As shown in Figure 8e, t_r and t_d were ~250 ns and ~300 ns, respectively. Both the rising and falling edges of the photocurrent were well-fitted to a single exponential function (red and orange curves in Figure 8e), with time constants for the rise (τ_r) and decay (τ_d) stages of 150 ns and 210 ns, respectively. The observation of only one decay time constant indicates that the fast recombination of free carriers dominates the decay of photocurrent.[31,53,54,56] The rise and fall time constants increased to 650 ns and 1.33 μs, respectively, as laser intensity decreased to 100 mW/cm² (Figure S9). No significant difference in response time constants was observed as the bias decreased to 2 V (Figure S10).

Averaging over 20 devices, the photodetectors had a rise time of 200–300 ns (τ_r=110–190 ns) and a fall time of 230–380 ns (τ_r=160–230 ns), respectively (Table S4). To the best of our knowledge, such a sub-microsecond response is not only the fastest result for reported CdS photodetectors (10^{-5} s),[57,58] but also much faster than for photodetectors made with other bottom-up semiconductor nanostructures,[30,31,59-61] as listed in Table S5.

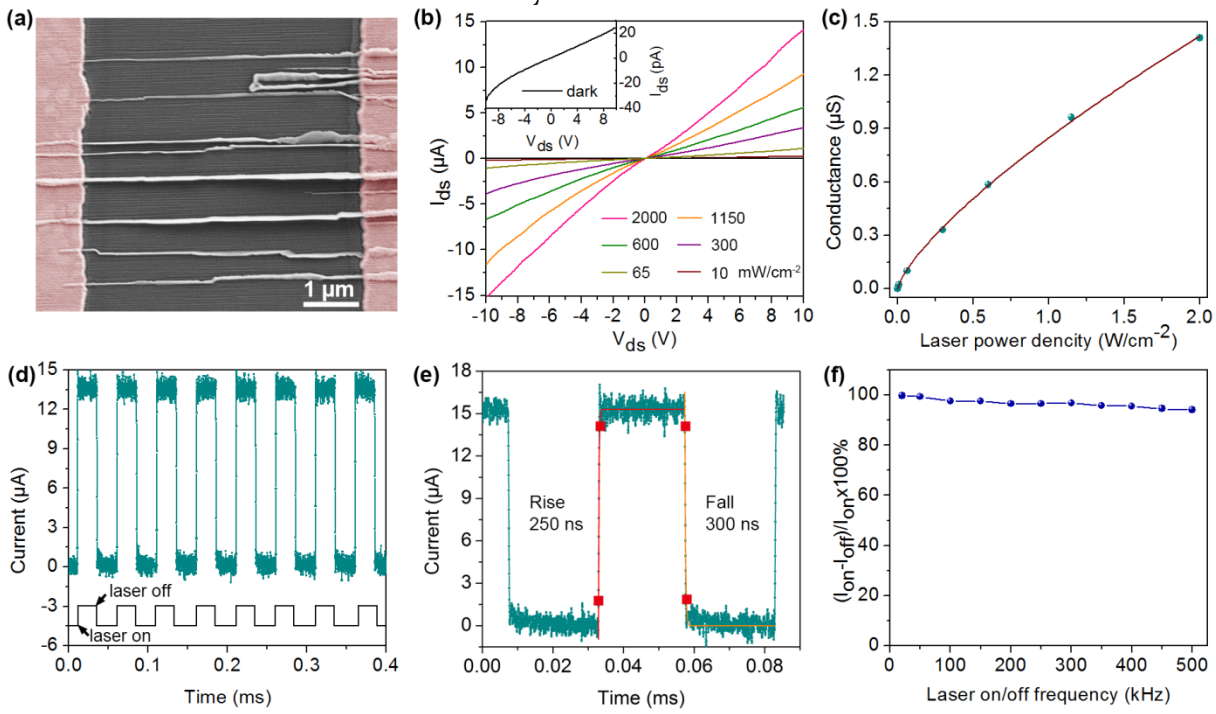

Figure 8. Performance of guided CdS-nanowall photodetectors. (a) SEM, (b) *I-V* curves under dark conditions (inset) and under illumination of a 405-nm laser with various power densities. (c) Conductance as a function of laser power density at a 10-V bias. (d, e) The photocurrent of CdS nanowalls under illumination of a 405-nm laser with an on/off frequency of 20 kHz and an intensity of 2 W/cm². The bias was 10 V. The recording time resolutions for panels (d) and (e) were 105 ns and 25 ns, respectively. The red squares in (e) indicate 10% and 90% points of the average peak value used for calculating the rise and fall time. The red (orange) line in (e) is the exponential fit of the rise (fall) edge. (f) The relative balance of photocurrent as a function of the frequency of the modulated laser.

Ultrafast response time, especially the ultra-fast recovery time (t_d), is very important for the fabrication of optoelectronic switches, light amplifiers, and counting circuits.[21,58] The 3-dB bandwidth (half power point, f_{3dB}=0.35/t_r) of these photodetectors was calculated to be 1.2–1.8 MHz, two orders of magnitude larger than the best results ever reported for CdS photodetectors (17.5 kHz),[32] further confirming the ultra-fast response speed of these detectors. Figure 8f shows that the relative balance of photocurrent ((I_{on}-I_{off})/I_{on}×100%) is always larger than 95% as the frequency of pulsed light approaches the limitation of our setup (500 kHz). The high 3-dB and relative balance of photocurrent indicate that these photodetectors could follow optical signals with on/off frequencies up to ~2 MHz.

The current responsivity (R_λ) and external quantum efficiency (EQE, or gain) of our photodetectors were calculated according to Equations (1) and (2), respectively,[52] where P_λ is the laser power density, S is the effective illuminated area and estimated by S=wdn in

term of nanowall width (w), electrode spacing (d) and number of nanowalls (n) (see also in the note of Table S4), h is the Planck's constant, c is the velocity of light, e is the electronic charge, and λ is the laser wavelength. Averaging over 20 devices (Table S4), these photodetectors had a current responsivity of 50–171 A/W and an EQE of 154–525, respectively.

$$R_\lambda = \frac{I_{on} - I_{off}}{P_\lambda S} \quad (1)$$

$$\text{EQE} = \text{Gain} = R_\lambda \frac{hc}{e\lambda} \times 100\% \quad (2)$$

The ultra-fast response and high gain of these photodetectors may result from multiple synergistic effects, including the features of guided nanowalls (high single-crystalline quality, small width), high excitation power density (2 W/cm^2) and bias voltage (10 V), and short electrode spacing (5 μm). According to the Rose model,[54,56,62] the discrete states in the forbidden zone, through which recombination of carriers is most likely to occur, can be divided into ground states (lying between the steady-state Fermi levels for electrons and holes, governing recombination rates and thereby free carrier densities) and shallow trapping states (responsible for observed response times exceeding the free electron lifetime) (Figure S11a). On the basis of this hypothesis, τ_R and the gain factor are defined by Equations (3) and (4),[53,56] respectively, where N_t/N is the ratio of trapped to free electrons. τ is the lifetime of free electrons and is given by Equation (5),[56] where v (10^7 cm/s at room temperature) is the thermal velocity of a carrier; s is the capture cross section of the capturing center, and n_c is the free electron concentration. τ_t is the transit time of an electron between electrodes and is given by Equation (6),[53] where L is the electrode spacing, V is the bias voltage.

$$\tau_R = \tau \frac{N_t}{N} \quad (3)$$

$$\text{Gain} = \frac{\tau}{\tau_t} \quad (4)$$

$$\tau = \frac{1}{vsn_c} \quad (5)$$

$$\tau_t = \frac{L^2}{\mu_e V} \quad (6)$$

On one hand, the high single-crystal quality of these nanowalls, as confirmed by TEM, XRD, and PL, indicates that the density of traps induced by defects was drastically reduced. Therein, a large n_c and small N_t/N are expected, leading to small τ and τ_R (fast response).[43,47] On the other hand, the demarcation lines between shallow trapping and ground states for electrons and holes shift toward the conduction and valence bands, respectively, with the increase of light intensity (Figure S11a).[54,56] As the demarcation lines diverged, more ground states were embraced. Consequently, increased n_c and decreased N_t/N are expected; hence, τ and τ_R become shorter at greater light intensity.

In addition to the high single-crystal quality of guided nanowalls and the high power densities of lasers, the small width of these nanowalls is another critical factor accounting for the sub-microsecond response. As shown in Figure S11b, the barrier height for surface electron-hole recombination (introduced by the pinning of the Fermi energy level at the surface of the nanostructure) is size-dependent and decreases significantly when the size of the sample is smaller than the critical value (depletion width, W_m).[52,63,64] Since most guided CdS nanowalls have widths of 15–35 nm, smaller than the W_m (42 nm), the barrier height is expected to be sufficiently low to allow a fast surface electron-hole recombination and hence a short τ_R.[62-64] In contrast to the ultra-fast response of guided CdS nanowall photodetectors, Figure S12 shows the photoconductive response of the nanobelt (~1 μm in width and ~400 nm in thickness) grown in a free-standing way under the same illumination. Although steady-state photocurrents are established within 10 μs of laser irradiation, the time required for these photocurrents to decay when optical excitation is interrupted extends to over 10 ms. The appearance of a slow decay tail is believed to be the result of the increased height of the recombination barrier for thick nanoribbons.[62-64]

The high bias voltage and short electrode spacing are the main reasons for the high gains of CdS nanowall photodetectors. According to Equation (6), the transit time of photo-generated electrons between electrodes is 5–13 ns if the measured μ_e is used for the calculation. Assuming that τ is 2 μs,[53,65] the estimated gain is 150–380 according to Equation (5), which is close to the EQE value, as expected (Equation (2)). Lastly, a faster response might be achieved by changing the 405-nm laser to a 490-nm laser since the best light response for CdS has been reported at this wavelength.[55]

■ CONCLUSIONS

We reported the bottom-up growth of guided CdS nanowalls with high single-crystal quality on flat or faceted sapphire surfaces. Unlike the epitaxial growth along certain crystal orientations on well-cut flat sapphires, graphoepitaxial growth is preferred on faceted sapphires with nanosteps and nanogrooves. Next, these self-aligned horizontal nanowalls were integrated in parallel into tri-gate FETs and photodetectors on a wafer scale without post-growth transfer or alignment steps. We have demonstrated that these tri-gate FETs are E-mode FETs with ultra-low off current (10^{-14} A) and a high on/off current ratio of 10^8 at a 1-V bias, four orders of magnitude higher than the best results ever reported for planar E-mode CdS FETs. This is because of the enhanced electrostatic control of the 3D tri-gate configuration. Therefore, this work indicates that guided semiconductor nanowalls with high single-crystal quality and appropriate size distribution open new opportunities for diverse high-performance 3D tri-gate FETs.

The nanowall photodetectors have impressive performance as well, including low dark currents, high

sensitivity, high gain (~10^2), and high relative photocurrent balance (>95%) for frequencies lower than 500 kHz, the shortest reported response time (~10^{-7} s), and the highest 3-dB bandwidth (~2 MHz) for photodetectors made of compound semiconductor nanostructures. Such high performance is mainly attributed to the unique features of a guided nanowall itself; therefore, this work also indicates that guided semiconductor nanowalls have potential applications in developing ultra-fast photodetectors. Finally, the high performance indicates that the electronic and optoelectronic properties of guided semiconductor nanowalls are not degraded by interaction with the substrate. In this regard, we proved that guided growth is very attractive for bottom-up integration of semiconductor nanostructures into high-performance 3D functional systems beyond the planar configuration.

■ ASSOCIATED CONTENT

Supporting Information

Experimental details, Figures S1–S14, Tables S1–S5, and calculation details (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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