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High-Gain 200-ns Photodetectors from Self-Aligned CdS-CdSe Core-Shell Nanowalls

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Abstract: One-dimensional core-shell heterojunction nanostructures have great potential for highperformance, compact optoelectronic devices, owing to their high interface area to volume ratio, yet their bottom-up assembly toward scalable fabrication remains a challenge. Here we report the sitecontrolled growth of aligned CdS-CdSe core-shell nanowalls by a combination of surface-guided vapor-liquid-solid (VLS) horizontal growth and selective-area vapor-solid (VS) epitaxial growth, and their integration into photodetectors at wafer-scale without postgrowth transfer, alignment or selective shell-etching steps. The photocurrent response of these nanowalls is reduced to 200 ns with gain of up to 3.8×10^3 and photoresponsivity of 1.2×10^3 A W⁻¹, the fastest response at such a high gain ever reported for photodetectors based on compound semiconductor nanostructures. The simultaneous achievement of sub-microsecond response and high-gain photocurrent is attributed to the virtues of both the epitaxial CdS-CdSe heterojunction and the enhanced charge-separation efficiency of the core-shell nanowall geometry. Surface-guided nanostructures are promising templates for wafer-scale fabrication of self-aligned core-shell nanostructures toward scalable fabrication of high-performance compact photodetectors from the bottom-up.

One-dimensional (1D) core-shell nanostructures are a promising alternative to thin-film for compact optoelectronics owing to their high interface to volume ratio between two extended phases.^{[1-} ⁶] Depending on the bandgaps and relative position of electronic energy levels of the involved semiconductors, core-shell nanostructures are divided into different types, dominated type-I, type-II, reverse type-I band alignments (or classified as p-n, n-n, p-p junctions).^[1,7,8] The different band alignments deliver different functions for practical applications. For instance, Zhang et. al.^[9] suggested that the photogenerated carriers in core-shell nanowires with a type-II band alignment are efficiently separated between the core and the shell, which extend both along the nanowire.^[1,4,10] Charge separation in these heterostructures is enhanced by shortening the diffusion length of minority carriers,^[5,6] and accordingly their photocurrent response. In type-I n-n core-shell nanowires,^[1,8] the shell is often used to passivate the surface of the core, aiming to improve the optical properties of nanowires. Realizing the substantial potential of core-shell nanostructures, however, requires predictable control over their composition, interface, direction, and shell-to-core alignment from the bottom-up.^[1-4] In particular, horizontal arrays are highly desirable toward scalable fabrication of nanodevices. However, deterministic assembly of freestanding core-shell nanostructures into horizontal arrays with controlled sites and shells remains a challenge. To date, although nanodevices based on core-shell nanostructures have been extensively studied, most of them were investigated at the single-nanostructure level^[2,3,10,11] or vertical arrays.^[12,13]

One possible option to have ordered core-shell nanostructures is to follow the postgrowth assembly that has been proposed for assembly of compositional-homogenous nanowires by aid of external forces.^[14-16] However, the alignment of postgrowth assembly is subject to thermal and dynamic fluctuations.^[14-16] Moreover, most postgrowth assembly approaches are incapable of controlling the shell length and location. Besides, selective shell-etching is usually involved after nanostructure growth in order to have electrode contact with the core region, which is another hurdle toward scalable fabrication. Although the postgrowth selective shell-etching based on a combination of lithography and wet chemical etching has been developed to expose the core in a lithographically defined region,^[10] this scheme exhibited disadvantages such as tricky control over etched shell thickness, damage on core surface, introduction of contamination, and so on.

In contrast to the postgrowth assembly, surface-guided horizontal growth offers a facile method to prepare aligned core-shell nanostructures with predictable aligned shells from the bottom-up, as we have recently reported.^[17] Horizontal growth was firstly observed during the growth of composition-homogeneous nanowires on atomic-flat single-crystal surfaces.^[18-26] Later, horizontal growth was also achieved on faceted substrates with periodic nanosteps or nanogrooves via the so-called "graphoepitaxy" (growth along relief features larger than lattice parameters).^[27-29] Since the first graphoepitaxial growth of horizontal GaN nanowires,^[29] a growing list of semiconductors has been succeeded in graphoepitaxy growth of nanowires, such as ZnO^[30] ZnSe,^[31] ZnTe,^[32] CdSe^[33] CdS.^[34] In the case of CdS, we found that a nanowall geometry has significant advantages over the nanowire geometry, enabling faster photodetectors and more efficiement field-effect transistors, owing to their 3-D tri-gate configuration. Would it be possible to combine the advantages of a core-shell 1-D heterostructure^[17] with those of a nanowall geometry^[34] in a single self-aligned nanostructure exploiting the phenomenon of graphoepitaxy?

Here we present a scheme that enables a site- and alignment-controlled growth of CdS-CdSe coreshell nanowalls on spontaneously nanofaceted sapphire surfaces. This scheme also offers a predictable control over shell length, site and alignment. Taking advantage of the self-aligned nanowalls and the site-controlled shells, their scalable integration into photodetectors is demonstrated, without postgrowth dispersion, transfer, alignment, and selective shell-etching steps. The photocurrent of these core-shell nanowalls exhibits simultaneously a sub-microsecond, high-gain response and high photoresponsivity owing to the virtues of both the epitaxial CdS-CdSe heterojunction and the enhanced charge-separation efficiency of the core-shell nanowire structure.

M-plane sapphire, i.e. α -Al₂O₃ (1010), is thermodynamically unstable, and forms periodic V-shaped nanogrooves upon annealing at elevated temperature.^[29] The slopes of the V-shaped nanogrooves are composed of R(1102) and S(1101) facets at an angle of 130° (**Figure 1**a). Figure

1b is the schematic drawing of typical experimental steps for the growth of CdS-CdSe core-shell nanowalls (see details in Supporting Information). As-received $M(10\overline{1}0)$ sapphire is first annealed at 1600 °C for 10 h to spontaneously form the desired nanogrooves. Gold nanoparticles are then deposited selectively on the annealed $M(10\overline{1}0)$ sapphire surfaces to serve as catalysts for the sitecontrolled growth. Aligned CdS nanowalls are grown by physical vapor deposition (PVD) using CdS powder as precursor. Thereafter, the sample is covered with a thin layer of polycrystalline Al_2O_3 by atomic layer deposition (ALD), followed by defining the area to be etched via photolithography, etching in a buffered oxide etch (BOE) solvent, and lift-off the remained photoresist with acetone. Next, the sample with selective-etched area is used to perform another PVD growth, this time using CdSe powder as precursor. Only the exposed nanowall surfaces are coated with CdSe layers via a surface-epitaxial growth owing to the selective-protection of the Al_2O_3 layer. Lastly, remained Al_2O_3 layer is removed by another etching in BOE solvent.

Scanning electron microscopy (SEM) revealed that the nanogrooves on annealed M (1010) sapphire surfaces have widths ranging from tens of nanometers (**Figure S1**, Supporting Information) to a few hundred nanometers (Figure 1c). Atomic force microscope (AFM) (Figures 1d and 1e) showed that these nanogrooves have heights of tens of nanometers. No aligned CdS nanostructures were observed on as-received M (1010) sapphire surfaces without nanogrooves (**Figure S2**, Supporting Information), whereas well-aligned high-density CdS nanowalls were obtained on the annealed M(1010) sapphire surfaces with nanogrooves (**Figure S3**, Supporting Information). These phenomena suggest that the nanogrooves on sapphire surfaces play the key role for the alignment of nanowalls. As-fabricated CdS-CdSe core-shell nanowalls are self-aligned along the nanogrooves with \pm [1120]_{Al₂O₃} directions (Figure 1f). The lengths of these nanowalls are ~50 µm for a 30-minute CdS-growth and the CdSe-shell lengths are 10 µm (**Figure S4**, Supporting Information). AFM image (Figures 1g and 1h) reveals that the heights of CdS-only regions usually less than 100 nm, while the heights of the core-shell regions exceed 200 nm. In general, the CdSe-shell thickness can be tuned from a few ten nanometers (**Figure S5**, Supporting Information) to a few hundred nanometers by

adjusting the CdSe-growth conditions (i.e. growth time or substrate temperature). It is worth emphasizing that this scheme also enables a predictable control over shell length and site from the bottom-up, in addition to the excellent alignment of nanowalls. For example, the length and site (~15 μ m away from the gold pad) of the CdSe-shells shown in Figure 1f were defined by a photolithography process before the CdSe-shell epitaxy (**Figure S4**, Supporting Information). Consequently, electrode contact can be laid down deterministically onto the cores and shells without postgrowth selective shell-etching, which is a crucial step toward scalable fabrication of nanodevices.

Two samples with different CdSe-growth times (different CdSe-thicknesses) were examined by grazing incidence X-ray diffraction (XRD). The diffraction peaks in each XRD pattern (Figure 2a) were indexed into a combination of hexagonal wurtzite CdS (purple, ICDD (International Center for Diffraction Data) No. 00-006-0314) and CdSe (orange, ICDD No. 01-070-2554) (Figure S6, Supporting Information). The relative intensity of CdSe peaks to CdS peaks in Sample-I is much smaller than that in Sample-II, indicating that the increase of CdSe growth time indeed resulted in an increase of CdSe-shell thickness. Compared with their ICDD peaks (purple and orange in Figure 2a), the shifts of CdS-peaks from both samples were negligible, indicating that the CdS-lattice distortion is very small after the CdSe-shell growth. The CdSe-peaks, however, shifted notably toward higher angles, and the CdSe-peaks from Sample-I with thinner CdSe-shells shifted more significantly than those of Sample-II. These observations suggested that the CdSe-lattice distortion was gradually relaxed with the increase of shell-thickness. The lattice spacing (d) was extracted from the XRD (see calculation details and Table S1 in Supporting Information) and compared with their ICDD data. The comparison yields a positive and negative Δd for CdS and CdSe (Table S1), respectively, indicating that CdS lattices undergone expansion whereas CdSe lattices undergone compression when they were brought together to form the core-shell nanowalls.

Cross-sectional transmission electron microscope (TEM) image (Figure 2b) shows that the angles of V-shaped nanogrooves are around 128°, very close to the 130° angle predicted by the atomic model (Figure 1a), hence the nanogroove surfaces are indeed composed of R{ $10\overline{1}2$ } and S{ $10\overline{1}1$ } lattice

planes. The nanostructure standing on the nanogrooves shows a well-defined nanowall geometry. Ten nanowalls were checked and they have heights of 130-410 nm and widths of 50-90 nm. EDS spectra collected from different locations (top left in Figure 2c) and the *in situ* electron energy loss spectrum (EELS) mapping (Figure 2c) revealed that Cd was uniformly dispersed throughout the nanowall cross section, whereas S was concentrated in the lower core region and selenium stayed near the nanowall surface (see more EELS mapping in Figure S7, Supporting Information), confirming the formation of CdS-CdSe core-shell heterostructure, as schematically shown in Figure 2d. In addition, more Se was detected on the nanowall top surface than that on the nanowall side surfaces, indicating CdSe had undergone a facet-selective growth.^[35,36] Possible reasons will be discussed later. Fast Fourier transformation (FFT) pattern (Figure 2e) revealed that these nanowalls have a wurtzite structure and a growth axis along the $[1\overline{1}01]_{CdS} \| [11\overline{2}0]_{Al_2O_3}$ direction. Besides, the CdS-FFT pattern is overlaped with the CdSe-FFT pattern, indicating their crystal lattice alignment is matched each other. Highresolution TEM (HRTEM) (Figures 2f, 2h) revealed that both the sapphire substrate and nanowalls possessed a single-crystalline quality after the growth, in agreement with the XRD results. Different from the atomic-sharp V-shaped CdS/sapphire interface, the CdS-CdSe interface is atomically continuous because of very small lattice mismatch between CdS and CdSe hexagonal phases. With the known crystallographic data and atomic models, the transversal and horizontal lattice planes of this nanowall are $\{11\overline{2}0\}$ and $\{1\overline{1}0\overline{2}\}$ planes, in parallel with $\{0001\}_{Al_2O_3}$ and $\{1\overline{1}00\}_{Al_2O_3}$ planes, respectively. Since the surface energy of top $\{1\overline{1}0\overline{2}\}$ surface is higher than that of lateral $\{11\overline{2}0\}$ surfaces,^[37] surface-adsorbed atoms from the CdSe vapor would diffuse preferentially to the more chemically active $\{1\overline{1}0\overline{2}\}$ surfaces,^[35] leading to the faster CdSe growth along the top surface than that along the sides, which explains the Se distribution in Figure 2c. Different from vertically aligned nanowires grown by lattice-match epitaxy,^[38] where the lattice match of nanowire with substrate existed along the nanowire height directions, the smallest lattice mismatch of horizontal nanowalls with sapphire was observed across the nanowall width with $[11\overline{2}0]_{CdS} \| [000\overline{6}]_{Al_2O_3}$ directions

(Figure 2e). This observation is consistent with other works,^[25] demonstrating that the nanogrooveguided growth is promising to hold a large tolerance for lattice mismatch between nanostructures and substrates.^[29,32,33] In Figure 2g, the selected inverse-FFT image shows that many misfit dislocations exist at the CdS-sapphire interfaces, which is reasonable considering the facts that CdS and sapphire are different crystal structures and the lattice mismatch along $[11\overline{2}0]_{CdS} \parallel [000\overline{6}]_{Al_2O_3}$ directions is up to -4.5%. The lattice fringes across the CdS-CdSe interface, however, are smooth and continuous (Figure 2i) because CdS and CdSe are the same hexagonal crystals with small lattice mismatch, and their crystal lattice alignment is matched each other (Figure 2e). Therefore, hetero-interfaces with few misfit dislocations were obtained, which is essential for reducing interface states and carrierstrapping centers, and thus increasing the recombination rate of free carriers as well as the photoninduced current.^[39,40]

Under 405-nm laser excitation, red emission was observed from the core-shell region of these nanowalls, whereas only green emission from the CdS-only region (**Figure 3**a). Spatially-resolved photoluminescence (PL) revealed that the PL spectrum from the green (red) emission region has a single-peak at 503 nm (708 nm) (Figure 3b). The emission peak energies (2.46 eV, 1.74 eV) are close to the room-temperature bandgaps of CdS and CdSe, respectively, therein they originate from the band-edge transitions of CdS and CdSe, respectively.^[41] The PL spectrum collected at the green-red junction exhibits two peaks, coming from the emission of CdS-core and CdSe-shell simultaneously. All nanowalls exhibit clean band-edge emission with no obvious trap-level emission observed across the entire nanowall, indicating the high quality of the nanowalls and few defects.^[42] 2-D PL-intensity mapping images (Figure 3c) revealed that only the CdSe 708-nm peak was detected from the coreshell region, although it is composed of CdS and CdSe compounds. The absence of CdS-green emission from the core-shell region is a result of the reconstructed bandgap diagram.^[43-48] We assume that the CdS and CdSe in these nanowalls are an n-type semiconductor due to background impurities/defects and the conductance band offset (ΔE_c) between them is quite small (<0.2 eV) since

although some theoretical results suggested that ΔE_c may larger than 0.2 eV.^[49] Therefore, although bulk n-n type CdS-CdSe system suggests a type-I band alignment, they can form a quasi-type-II band alignment through Femi-level alignment owing to the small ΔE_c and the low effective mass of electrons.^[43-48] Consequently, photogenerated electrons are commonly assumed to extend along the entire nanostructure, whereas holes are predicted to be strongly confined in the valence band of the CdSe shell due to the large valence band offset (ΔE_v >0.5 eV) and high effective mass of holes.^[48]

The above characterizations confirmed that self-aligned CdS-CdSe core-shell nanowalls with controlled site, micro-scale length, high density and predictable shells were obtained on insulating sapphire surfaces. Consequently, photodetectors can be fabricated in a scalable manner (Figure S8, Supporting Information) without postgrowth transfer, shell-to-core alignment or selective shelletching steps, and that devices can be made of aligned arrays of many nanowalls. Figure 4a shows the SEM image of a representative photodetector made of 13 CdS-CdSe core-shell nanowalls, in which electrodes were deposited selectively onto the cores and shells to form Ohmic contacts. Figure 4b plots the current-voltage (I-V) curves under dark condition and illumination of 405-nm light with different intensities as bias voltage was applied onto the CdS-cores. All curves showed a wellexpressed rectification action due to the heterojunction barriers, demonstrating that these CdS-CdSe heterojunctions behave as well-defined diodes. The on/off current ratio is on the order of 10^2 (Figure **S9**, Supporting Information) when the bias swept from 5 V to -5 V. Figure 4c further revealed that these diodes have a very poor photovoltaic response to the 405-nm light,^[50] with small open-circuit voltages (V_{oc}) and short-circuit currents (I_{sc}). As expected, V_{oc} and I_{sc} depend logarithmically and linearly (inset in Figure 4c), respectively, on the light intensity.^[10] Under illumination, the ideal diode equation can be expressed as $\ln(I_{sc}) = qV_{oc}/NkT + \ln(I_0)$,^[10] where q is the electronic charge, N is the diode ideality factor, k is the Boltzmann constant, and I_0 is the reverse saturation current. Linear fitting of a plot of $\ln(I_{sc})$ versus V_{oc} (Figure S10, Supporting Information) yields a N and I_0 of 1.29 and 561 pA, respectively. The N value is close to the value of an ideal Schottky junction (N=1), indicating the high quality of the CdS-CdSe heterojunctions.

High response speed and high photocurrent gain play key roles for the development of highperformance photodetectors.^[51-54] Unfortunately, a large gain often reduces the response speed, or vice versa, as a result of the exciton recombination at the surface and bulk of nanostructures.^[51] The photocurrent of these detectors follows the square change of incident light intensity at the submillisecond level (Figure 4d), suggesting a sub-microsecond photocurrent response. The on-current and off-current in each cycle were stable at an order of 10⁻⁵ A and 10⁻⁷ A, respectively, resulting in a 10^2 on/off current ratio, demonstrating the excellent repeatability of the photodetectors. However, the off-current is still relative high and on/off current ratio is low, In order to determine the rise and fall times accurately, the photocurrent-record time interval was reduced to 35 ns (Figure 4e) from 105 ns (Figure 4d). The rise and fall edges of the photocurrent were well-fitted by a single-exponential function (Figure 4e), respectively, with time constants of ~200 ns for both the rise (τ_r) and decay (τ_d) stages. The observation of only one decay time constant for both rise and decay stage indicates that the fast recombination of free carriers, instead of the slow recombination of trapped carriers, dominates the photocurrent decay.^[33,55-57] Statistic of 10 devices gives $\tau_r = 170-250$ ns and $\tau_d = 160-$ 330 ns, respectively (Table S2, Supporting Information). The 3-dB bandwidth (half power point, $f_{3dB}=0.35/\tau_d$)^[58] of these photodetectors are 1.4–2.1 MHz, suggesting that these photodetectors could follow the changes of optical signals with on/off frequencies approaching 2 MHz. For example, Figure 4f shows that the relative balance of photocurrent ((I_{on}-I_{off})/I_{on}×100%) is always larger than 95% as the frequency of the modulated light approaches 500 kHz. Compared with bias voltage, light intensity has a more significant contribution to the sub-microsecond response. For example, the photocurrent remains a submicrosecond response when bias voltage was reduced to 1 V (Figure S11, Supporting Information). In contrast, both the rise and fall times reduced rapidly from ~2 µs to ~300 ns as the light intensity raised to $\sim 100 \text{ mW cm}^{-2}$, thereafter they approach very slowly to a plateau at ~200 ns (Figure 4g).

The gain factor (η) denotes the number of detected electrons per incident photon, and is determined by $\eta = Rhc(e\lambda)^{-1}$,^[59] where *R* is the photoresponsivity, *h* is the Planck's constant, *c* is the velocity of

light, *e* is the elementary charge, and λ is the laser wavelength. *R* is determined by $R=I_{ph}/PS$, where I_{ph} is the net current, *P* is the light intensity, *S* is the effective illuminated area. Figure 4h plots the light-intensity dependent *R* and η at 10-V bias. It is clear that both *R* and η decreases with increasing *P* and reach maximum values of $R=3.6\times10^3$ A W⁻¹, $\eta=1.1\times10^4$ at the lowest P=54 mW cm⁻². A quantitative fitting of *R* yields a power-law decrease, $R\propto P^{a-1}$, with the fitting parameter a=0.64, which is close to the reported values (a=0.71-0.79),^[39,40,60] indicating an enhanced scattering or recombination rate of hot carriers as their density increases at higher light intensity.^[39,40,60] It is worth emphasizing that *R* and η are still as high as 1.3×10^3 A W⁻¹ and 4.4×10^3 , respectively, at the highest light intensity we performed, where the shortest response time of 200 ns was achieved. Averaging over 10 devices (**Table S2**, Supporting Information) yields $R=1.2\times10^3$ A W⁻¹ and $\eta=3.8\times10^3$, respectively, at P=740 mW cm⁻² and 10 V bias.

As listed in **Table I**, the sub-microsecond response of these core-shell nanowalls is similar to the response of the guided CdS nanowalls, being the fastest results ever reported for photodetectors based on bottom-up compound semiconductor nanostructures.^[31,61-63] The photoresponsivity and gain of the core-shell nanowalls, however, are one order of magnitude higher than those of pure CdS nanowalls. The main reasons for the simultaneous realization of sub-microsecond response and high-gain photocurrent (efficiency) include the improved carrier separation enabled by the quasi-type-II band alignment of these nanowalls (see the discussion about the PL results) and the enhanced charge-injection efficiency offered by the high-quality epitaxial heterojunctions, the relative high illumination, and high bias voltage. The enhanced charge-injection efficiency has a semiquantitative description with the Rose model.^[56,57] Rose assumed that there is a high concentration of levels with a broad energy distribution (discrete states) in the forbidden gap of semiconductors, and they can be divided into ground states (major recombination traffic) and shallow trapping states (cause the observed response time to exceed the free-electron lifetime) (Figure 4i).^[57] Where n_e/n is the ratio of trapped to free electrons, τ is the lifetime of a free electron and is given by $\tau = 1/vsn_e^{[57]}$ in terms of the

thermal velocity of free carriers (v), the capture cross sections of ground states for electrons (s),^[55] and the free electron concentration (n_c) . In general, τ is substantially constant at room temperature under certain illumination once the semiconductor nanostructures were prepared since s and n_c depend on the method and conditions that used to produce the nanostructure.^[55-57] Owing to the single-crystal quality of nanowall and the high-quality CdS-CdSe interface, as confirmed by XRD, HRTEM, PL and I-V curves, the defect density is expected to be low, leading to a low number of trapped electrons (n_t) . More importantly, the quasi-type II bandgap alignment (Figure 3d) and the abrupt epitaxial interfaces are expected to enhance the carrier separation efficiency; consequently, raising the number of free electrons (n). The suppressed n_t and increased n eventually result in the ultra-fast light response at room temperature. The light intensity dependent response time also has an explanation with the Rose model. With the increase of light intensity, the demarcation lines between shallow trapping and ground states for electrons and holes shift toward the conduction and valence bands, respectively.^[56,57] The shift of demarcation lines will bring new centers into the role of ground states, leading to an increased n_c and n. Consequently, τ and τ_R become shorter at greater light intensity. The photoresponsivity and gain are also expressed as $R = [e\alpha t\lambda/hc]\tau_1/\tau_t$ and $\eta = [\alpha t]\tau_1/\tau_t$, [39,40] respectively, in terms of the absorption coefficient (α), the nanowall height (t), and the ratio of the lifetime of minority carriers (τ_1) to the transit time of majority carriers (τ_t). Considering that $\tau_t = L^2/\mu V$, where L is the electrode spacing, μ is the electron mobility, V is the bias, the photoresponsivity and gain increase linearly with increasing applied bias voltage. As light intensity increases, Auger recombination processes will be introduced and carriers scattering will be enhanced.^[39,40] The Auger recombination processes lead to reduced τ_1 while the enhanced carriers scattering results in an increased τ_t ,^[39,40] which explains the reduced photoresponsivity at higher light intensity in Figure 4h.

In summary, a facile approach is presented for site-controlled growth of aligned CdS-CdSe coreshell nanowalls based on the combination of graphoepitaxially guided VLS growth and selective-area VS epitaxial growth. This approach offers not only a self-alignment of nanowall themselves, but also a site- and length-controlled shells from the bottom-up, which paves the way to scalable fabrication

of nanodevices. As an example, photodetectors were fabricated in a scalable manner without postgrowth alignment, transfer, or shell selective-etching steps. A sub-microsecond response and high-gain photocurrent as well as high photoresponsivity were achieved simultaneously from these photodetectors. Lastly, the proposed approach is not limited to the CdS/CdSe system. In principle, different core-shell heterojunctions can be obtained by changing the core or the shell composition. Therefore, this work indicates that surface-guided growth can be extended to produce horizontally-aligned core-shell heterostructures for scalable fabrication of high-performance devices from the bottom-up.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Figure 1. Surface-guided CdS-CdSe core-shell nanowalls. (a) Atomic model of $M(10\overline{1}0)$ sapphire before (left) and after (right) annealing. Red and cyan balls are oxygen and aluminum, respectively. (b) Schematic drawing of experimental steps. (c) SEM, (d) AFM and (e) height of the nanogrooves self-formed on annealed $M(10\overline{1}0)$ sapphire surface. (f) 45°-titled SEM of CdS-CdSe core-shell nanowalls. (g) 3D AFM image of CdS-CdSe nanowalls. (h) Representative height across the CdS-only and CdS-CdSe core-shell region.



Figure 2. Structure characterization of surface-guided CdS-CdSe nanowalls. (a) XRD. The CdSegrowth time for Sample-I and Sample-II is 5 min and 15 min, respectively. The red and green dashed lines indicate the peak position of wurtzite CdSe (orange) and CdS (purple) structure, respectively. (b) Cross-sectional TEM image. (c) EDS spectra collected from the three locations marked with crosses in (b) and electron energy loss spectrum (EELS) mapping of Cd, S, Se, respectively. (d) Schematic drawing of the CdS-CdSe core-shell nanowall standing on the nanogroove. (e) FFT pattern of (b). HRTEM views near the CdS/sapphire interface (f) and CdS/CdSe interface (h). The dashed line in (h) indicates the boundary between CdS and CdSe. (g) Constructed inverse-FFT image along the nanowall width for the area in (e), pink arrows indicate the misfit dislocations. (i) Constructed inverse-FFT image along the nanowall height for the area in (h).



Figure 3. Optical properties of surface-guided CdS-CdSe core-shell nanowalls. (a) Real-color emission optical image of nanowall arrays under 405-nm laser illumination. The image was filtered with a 405-nm notch filter. (b) Intensity-normalized PL spectra when single nanowall was excited at different locations (marked with crosses in a) with a focused 325-nm laser beam. (c) 2D PL-intensity mapping for the green and red peaks, respectively. The cyan dashed line indicates the junction position between the core-only and core-shell regions. (d) Bandgap diagram of CdS-CdSe system before (upper) and after (bottom) Fermi-level alignment. Photogenerated electrons are not confined whereas holes are tightly confined to the CdSe shells.



Figure 4. Optoelectronic properties of surface-guided CdS-CdSe core-shell nanowalls. (a) SEM image of photodetector, false color was added onto one nanowall to show the CdS-only region (cyan) and CdS-CdSe core-shell region (pink). (b) *I-V* curves under dark condition (black) and 405-nm light illumination with different intensities. (c) Zoom-in view of (b) in the range of ± 0.2 V, inset is the plot of V_{oc} and I_{sc} as a function of light intensity. (d, e) Photocurrent response under illumination of 405-nm light at 10-V bias. The on/off frequency of the light is 10 kHz, and intensity is 740 mW cm⁻². The time interval for the current acquirement is 105 ns (d) and 35 ns (e), respectively. The orange and pink lines in (e) are the exponential fitting for the rise and decay edges, respectively. (f) Frequency-dependent balance of photocurrent at 10-V bias, and 740 mW cm⁻². (g) Light intensity dependence of rise and fall time at 10-V bias. (h) Light intensity dependence of photoresponsivity (pink) and gain factor (cyan) at 10-V bias. (i) Model showing the continuous distribution of discrete states. Increased

rate of excitation adds more states to the ground states and thereby leads to the shorter lifetime of free carriers. The light yellow and orange regions represent the shallow trapping states for electrons and holes, respectively. The cyan region corresponds to the ground states. The red and green arrows represent the thermal equilibrium process of trapped carriers and recombination of free carriers, respectively. Adapted with permission from Ref. [55].

Table 1. Photoconductivity performance based on different semiconductor nanostructures.

	Light [nm]	Intensity [mW cm ⁻²]	Bias [V]	I _{off}	I _{on}	$ au_{ m r}$	$ au_{ m d}$	<i>R</i> [A W⁻¹]	Gain	Ref.
CdS NW ^{a)}	400	_	2.0	<2 pA	100 nA	15 µs	15 µs			[64]
CdSe NW ^{a)}	473	1500	2.0	10 ⁻⁷ A	3.5 µA	2—3 µs	2—3 µs	14—347	36—911	[33]
ZnSe NB ^{b)}	405	13	30.0	10 fA	10.7 pA	70 ms	0.2 s			[31]
ZnO NW ^{a)}	370	_	5.0	29 µA	34 µA	100 µs	360 µs			[62]
ZnS NB ^{b)}	320	_	5.0	10 ⁻¹⁴ A	0.6 pA	2.57 ms	1.99 ms			[65]
GaSb/GaIn Sb NW ^{a)}	1550	_	1	_	<0.5 µA	2 ms	3.7 ms	10 ³	8.5×10 ⁴	[63]
CdS-CdSe NB ^{b)}	515	3.5	4.0	pА	1 µA	30 ms	90 ms	10 ³	104	[66]
CdS-CdSe axial NW ^{a)}	480— 640	2.86	1.0	10 ⁻¹² A	10 ⁻⁷ A	68 µs	137 µs	118	3.1×10 ²	[67]
Guided CdS NW ^{c)}	405	2000	10.0	10 ⁻⁸ A	10 ⁻⁶ A	<300 ns	<400 ns	50—171	154—525	[34]
This work	405	740	10.0	10 ⁻⁷ A	10 ⁻⁵ A	<250 ns	<330 ns	1.2×10 ^{3 d)}	3.8×10 ^{3 d)}	

^{a)}NW is Nanowire; ^{b)}NB is nanobelt; ^{c)}NW is nanowall; ^{d)}These values are an average over 10 photodetectors.

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A facile approach is proposed for the site-controlled synthesis of horizontally aligned CdS-CdSe core-shell nanowalls with abrupt epitaxial interfaces and predictable aligned shells on insulating sapphire surfaces, and accordingly a wafer-scale fabrication of high-gain 200-ns photodetectors without postgrowth transfer, alignment or selective shell-etching steps.

Keyword: CdS, CdSe, core-shell, photodetector, nanostructure

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High-Gain 200-ns Photodetectors from Self-Aligned CdS-CdSe Core-Shell Nanowalls

ToC figure



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4 Supporting Information

High-Gain 200-ns Photodetectors from Self-Aligned CdS-CdSe Core-Shell Nanowalls

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13 Experimental Section

14 Substrate preparation. As-received well-cut double-polished M ($10\overline{1}0$) sapphire (Roditi 15 International Corporation Ltd, England) was annealed at 1600 °C for 10 h. After annealing, V-shaped 16 nanogrooves were obtained on the sapphire surface. In order to have selective-deposited gold 17 catalysts for the growth, the annealed sapphire was firstly marked (either with 5-µm line arrays or $3 \times 30 \ \mu m^2$ pads) with a negative photoresist (NR9-1000PY) by a standard UV photolithography, 18 19 followed by electron-beam-deposition of 5-Å-thick gold film. After lift off the photoresist layer with 20 acetone, the gold film was dewetted at 550 °C for 10 min to form gold nanoparticles before being 21 used for growth.

22 *Nanowall growth.* The growth of guided CdS nanowalls was performed in a two-zone horizontal tube 23 furnace with rapid heating ability. Both CdS powder and sapphire substrate were connected with 24 magnets in order to adjust their position by magnet force (Figure S12, Supporting Information). In a 25 typical synthesis, CdS power (0.12 g, 99.99%, Sigma-Aldrich) evaporated at 860 °C serves as the 26 precursor and high-purity N₂ was used as the carrier gas. The sapphires with Au catalysts maintained 27 at 560-600 °C were used for the collection of vapors from the source. The growth usually lasts 20-28 40 minutes under 300-400 mbar in order to have a micro-scale length. After CdS growth, 25-nm 29 Al₂O₃ layer was deposit over the whole substrate by atomic layer deposition (ALD, Fiji F200) at 30 250 °C. A second photolithography was then performed to define the area to be etched. The etching

was performed by dipping the sample into a buffered oxide etch (BOE) solution (6:1 with surfactant,
JT Baker) for 28 seconds at room temperature. After removing the photoresist, the selective-etched
sample was then used to perform another PVD process in the presence of CdSe vapors. The
temperature of CdSe powder and sapphire substrate were set to 750 °C and 500 °C, respectively, and
the CdSe growth time is various from 5 min to 20 min in order to have different shell thickness. Last,

6 the rest Al₂O₃ layer was etched by performing another etching in BOE solution for 30 seconds.

Structural characterization. The morphology of as-grown samples was observed by SEM (Supra S5VP FEG LEO Zeiss). Grazing incidence XRD was performed on Rigaku ULTIMA III (λ = 1.54 Å, Cu-Ka9) in order to substrate the signals from the sapphire substrate. For analyses of the crystallographic structure, orientation, and epitaxial relationships of the nanowalls, a focused ion beam (FIB, FEI Helios 600 Dual Beam microscope) was used to cut thin (50–100 nm) slices across nanowalls, after which they were observed under a high-resolution transmission electron microscope (HRTEM, FEI Tecnai F20). More details are provided in our previous paper.^[R1]

Nanodevice fabrication. A photolithography mask was designed to define an electrode pattern compatible with the catalyst pattern of the guided nanowalls. After growth, sapphires with ordered nanowalls were first marked by standard photolithography. Next, Cr/Au (10/400 nm) metal layers were laid down as electrodes using electron beam deposition (SELENE ODEM). After lift-off in acetone, photodetector arrays were obtained. Before electronic and optoelectronic measurements, the device was annealed at 300° for 3 h in a N₂ atmosphere in order to obtain a good contact condition between the nanowalls and metal electrodes.

Electronic and optoelectronic measurements. All measurements were done under high vacuum (~10⁻
⁴ Torr) at room temperature using a Janis ST-500 probe system with a Keithley 4200-SCS. A 405-nm
laser was used to illuminate the device and the light intensity was adjusted by a metallic neutral
density filter (Thorlabs). For on/off current measurements, the 405-nm laser was periodically turned
on and off (modulated) by an acousto-optic modulation (AOM) system with a response time of ~30

- 1 ns. The bias voltage was set to 10 V in order to obtain a high signal-to-noise ratio for most on/off
- 2 measurements.
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Figure S1. AFM image and height profile of annealed $M(10\overline{1}0)$ sapphire surfaces with nanogroovewidth of tens of nanometers.

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- **Figure S2**. SEM images of CdS nanowalls on well-cut flat $M(10\overline{1}0)$ sapphire. No prefered directions
- 14 were identified.



Figure S3. SEM image of guided CdS nanowalls on annealed $M(10\overline{1}0)$ sapphire surfaces with a high-density.



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5 **Figure S4**. 30° -titled SEM images of guided CdS-CdSe core-shell nanowalls on annealed M($10\overline{1}0$) 6 sapphire surfaces from gold strips.



8 Figure S5. SEM images of guided CdS-CdSe core-shell nanowalls with thinner CdSe-shells.



Figure S6. The observed peaks in each XRD specturm were indexed into a combination of hexagonal wurtzite CdS (purple, ICDD No. 00-006-0314) and CdSe (orange, ICDD No. 01-070-2554).



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- 2 Figure S8. Digital photograph of CdS-CdSe nanowall photodetectors fabricated in a scalable manner
- 3 using microfabrication technique. The size of the sapphire substrate is 8×8 mm²



4 5 Figure S9. Re-plot of the *I-V* curve at 54 mW cm⁻² illumination in logarithmic scale shows the on/off 6 current ratio is 10^2 .



Figure S10. Plot of $\ln(I_{sc})$ vs V_{oc} . The fitting yields reverse saturated current I_0 =561 pA, and ideality 9 factor *N*=1.29.





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Figure S11. Photocurrent under illumination of a 20-kHz 405-nm laser with 740 mW cm⁻² light density at 1-V bias. The rise and fall time constants are around 250 ns and 540 ns, respectively. They are calculated by fitting the rise and fall edges with a single exponential function.

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8 Figure S12. Schematical growth setup and procudure. The table lists the experimental parameters for

10

- 11
- 12 **Table S1**. Interplanar spacing (d_{hkl}) from XRD, JCPDS card, percentage of variation of d, and
- 13 FWHM.

⁹ the growth.

	{hkil}	d _{xRD} [Å]	d _{JCPDS} [Å]	Δ <i>d</i> [%]	Peak shift [°]	FWHM [°]
	а	4.1438	4.1365	0.18	-	_
	С	6.7240	6.7160	0.12	-	_
CdS ^{a)}	1010	3.5887	3.5823	0.18	-0.05	0.183
	0002	3.3620	3.358	0.12	-0.04	0.241
	1011	3.1660	3.1608	0.16	-0.05	0.205
CdSe ^{a)}	а	4.2835	4.2982	-0.34	-	-
	с	6.9752	7.0084	-0.47	-	-
	1010	3.7096	3.7224	-0.34	0.08	0.319
	0002	3.4876	3.5042	-0.47	0.11	0.392
	1011	3.2752	3.2874	-0.37	0.10	0.337

^{a)}XRD information was extracted from Sample-II only since the CdSe-peaks from Sample-I are too weak and the CdS peaks from both samples are very close to each other.

The lattice plane spacing $d_{(hkil)}$ of wurtzite CdS is related to the lattice constants *a*, *c* and the Miller indices (*hkil*) by Equation (S1).^[R2] The lattice constant *a* for {1010} planes is calculated by Equation (S2), where θ is obtained by fitting the {1010} peak in the XRD pattern with a Gauss function, λ =1.54 Å is the wavelength of the X-ray. The lattice constant *c* for {0002} planes is calculated by Equation (S3), where θ is obtained by fitting the {0002} peak in the XRD pattern with a Gauss function. Therefore, the calculated lattice constants are *a*=*b*=4.1405 Å and *c*=6.7190 Å.

$$10 \quad \frac{1}{d^{2}(hkl)} = \frac{4}{3} \left(\frac{h^{2} + hk + k^{2}}{a^{2}} \right) + \frac{l^{2}}{c^{2}}$$

$$11 \quad a = \frac{\lambda}{\sqrt{3} \sin \theta}$$

$$12 \quad c = \frac{\lambda}{\sin \theta}$$
(S1)
(S2)
(S2)
(S3)

$$\frac{12}{13} \quad c = \frac{1}{\sin\theta}$$

1 2

No. of Nanowalls	$[ns]^{a)}$	τ _d [ns] ^{a)}	 [MHz] ^{b)}	on/off ratio	Photoresponsivity [A W ⁻¹]	Gain [10 ³]
14	245	330	1.4	181	1015	3.1
11	246	193	1.4	110	1204	3.7
10	221	201	1.6	181	1334	4.1
7	204	162	1.7	102	1591	4.9
13	205	168	1.7	281	1598	4.9
13	170	193	2.1	99	1077	3.3
15	171	172	2.0	138	1128	3.5
17	210	187	1.7	121	1278	3.9
10	204	162	1.7	182	1114	3.4
10	244	220	1.4	123	1221	3.7
Average	212	200	1.7	152	1256	3.8

 Table S2. Performance summary of 10 photodetectors

^{a)} τ_r and τ_d are the rise and decay time constant, which are defined by the time interval between 1/e and (1-1/e) of maximum photocurrent; ^{b)} $f_{3dB}=0.35/\tau_r$ is the 3-dB width.

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